Monolithic GaAs Dual-Gate FET Variable Power Amplifier Module*

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ABSTRACT

The design, fabrication, and microwave performance of a monolithic four-stage GaAs dual-gate FET amplifier are described. A linear gain of 23 dB with 250 mW output power has been measured at 18 GHz. The highest power obtained was 500 mW with 21 dB gain at the same frequency. By varying the second gate bias voltage, a dynamic gain control range of more than 60 dB has been observed. The chip size is 6.45 mm x 2.1 mm x0.1 mm.

INTRODUCTION

Single gate monolithic GaAs FET power amplifiers are being developed at several laboratories for phased-array radar, EW, and satellite communications. For some applications, it is desirable to vary the output power without changing the insertion phase over a wide dynamic range. The GaAs dual gate FET is ideally suited for this purpose as described in [1]. This paper reports the monolithic integration of a four-stage GaAs dual-gate FET amplifier with totally integrated bias networks. Up to 500 mW output power with 21 dB have been obtained at 18 GHz while a dynamic gain control of more than 60 dB has been observed by varying the second gate bias voltage.

CIRCUIT DESIGN

The circuit topology of the four-stage amplifier is shown in Figure 1. For the circuit design, realistic device models with cascode-connected common-source, common-gate stages as described in Reference 1, were obtained by comparing measured device S-parameters with the models generated from computer optimization. The gate widths of the four FET's are 240 μm, 240 μm, 480 μm and 1200 μm. High impedance transmission lines with a characteristic impedance of ~80 ohms were used along with silicon nitride MIM capacitors for impedance matching. Multiple transmission lines were used in the third and fourth stages to ensure more uniform phase and amplitude distributions of the input and output signals of the FET's for minimizing gain degradation. Computer simulation of this amplifier shows that a gain in excess of 20 dB can be obtained from 17 GHz to 19 GHz. The drain bias network uses quarter wavelength transmission lines connected to 13-pF shunt capacitors. The first and second gate biasing networks include resistors for bias decoupling and low-frequency stabilization. In order to minimize the phase change when the control voltage is changed, the second gates of the FET's are capacitively terminated to ground [1].

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FET DESIGN AND CIRCUIT LAYOUT

To achieve stable operation of dual-gate FET's, it is desirable to distribute the capacitive termination of the second gate. Consequently, we have adopted a Pi gate design for all the FET's. The individual gate fingers are 60 μm for both the first and the second gates. Each of the second gate feeds is positioned between two drain pads. Each second gate finger is connected to a 1.3 pF MIM capacitor. For stable high frequency operation, very low source lead inductance and good grounding of the second gate capacitors are essential. We have used individual via holes for each of the FET's source pads to satisfy the first conditions. The second requirement is satisfied by connecting each of the second gate capacitors to the source pads with air-bridges. Figure 2 gives a detailed view of an FET section. Since the gain of a dual-gate FET falls 12 dB per octave, the definition of a small gate length is even more crucial than for single gate FET's. For the present application a gate length of 0.4 to 0.5 μm was chosen. The capacitors used in the circuit are of two types. MIM silicon nitride structures are used for the medium and large capacitors. For the input and output of the last stage, the capacitance to ground of large pads are used. The size of these two pads enables very uniform distribution of the tuning elements of each FET section for maximizing gain and power.

CIRCUIT FABRICATION

Figure 3 is a photograph of the chip after completion of front side processing. The chip size is 6.45 mm X 2.1 mm X 0.1 mm and contains four dual-gate FET's and all series and shunt capacitors and transmission lines. The substrates used in this work are two inch diameter Cr-doped LEC slices. The active layer is grown by arsenic trichloride vapor phase epitaxy and are anodically thinned. The material

structure comprises a 1 μm undoped buffer layer and a 0.3 μm n-GaAs active layer doped to about 2.5 x 10^{17} cm^{-3} with Si. Following epitaxial layer growth, mesas are etched to isolate FET's and to define 100 ohms resistors used in the first gate biasing network. Au-Ge/Ni ohmic contacts are then formed by lift-off and alloyed. This step also defines 10, 20 and 50 ohm resistors used in the first gate biasing network. The 0.4 to 0.5 μm gate pattern is written in pmma by electron beam lithography. Three different fields are used to define respectively the two 240 μm FET's, the 480 μm and the 1200 μm FET's. The GaAs is etched again down to the I_{sat} value and Ti/Pt/Au gates are then fabricated by evaporation and lift-off. Another Au based layer is evaporated and lifted-off to produce capacitor bottom plates, inductors and source grounding areas. MIM capacitors are fabricated and plated gold air bridges are formed to contact FET sources and capacitors top plates. The transmission lines and all pads are also plated with 3 μm of gold at the same time. The slice is then lapped to 100 μm and grounding vias are etched by reactive ion etching. A total of 48 vias are used, one under each FET source pad and three under each bypass capacitor. The cross section shown in Figure 4 has been done at the source pad level and illustrate the high aspect ratio obtained by RIE and the 10 μm thick plated gold heatsink interconnecting all the vias.

MICROWAVE PERFORMANCE

The completed amplifier chip was mounted in a gold plated copper carrier for microwave characterization. Input/output 50-ohm lines on alumina substrates were used for connecting to the test chip. Figure 5 shows the measured gain-frequency response of the four-stage amplifier. With the dc bias voltages shown and with 0 dBm input, a gain of ~20 dB was obtained across the 17 to 19 GHz range. With an increased drain voltage, an output power of 500 mW with 21 dB gain and 14.9% power-added efficiency were achieved at 18 GHz. The linear gain was 23 dB with 250 mW output. It is to be noted that, due to the optimum bias network design, unconditionally stable operation has been obtained.

CONCLUSION

Multi-stage, monolithic amplifier implementation of GaAs dual-gate FET's has been demonstrated in the Ku/K band frequency range. The four-stage amplifier, with a chip size of 6.45 mm x 2.1 mm x 0.1 mm, has achieved a maximum output power of 0.5 W at 18 GHz with at least a 60 dB dynamic gain control range. This amplifier chip will find applications in satellite communication systems requiring variable power amplifier modules with small size, light weight, and solid-state reliability.

REFERENCE

[1] B.M. Kim, H.Q. Tserng, and P. Saunier, "GaAs Dual-Gate FET for Operation up to K-Band," IEEE Trans. Microwave Theory and Tech., Vol. MTT-32, no. 3, March 1984.

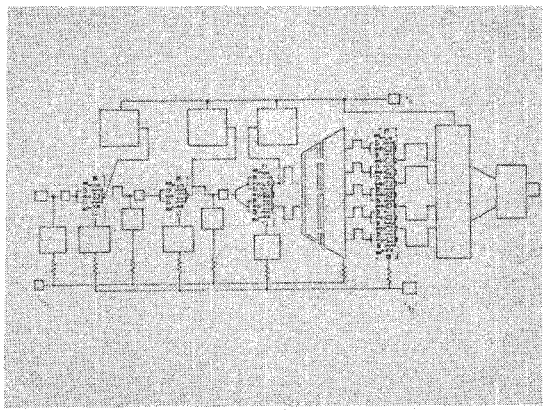

Figure 1. Dual-Gate Amplifier Circuit Topology

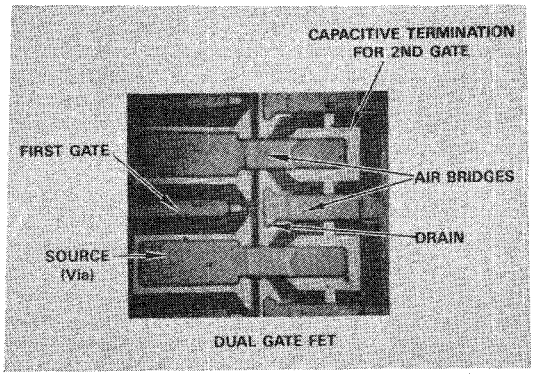

Figure 2. Detailed View of a Dual-Gate FET

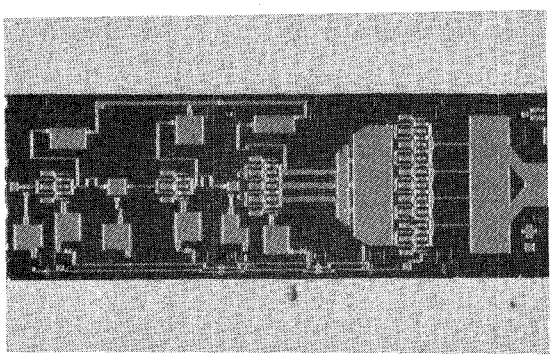

Figure 3. Photograph of the Completed Amplifier

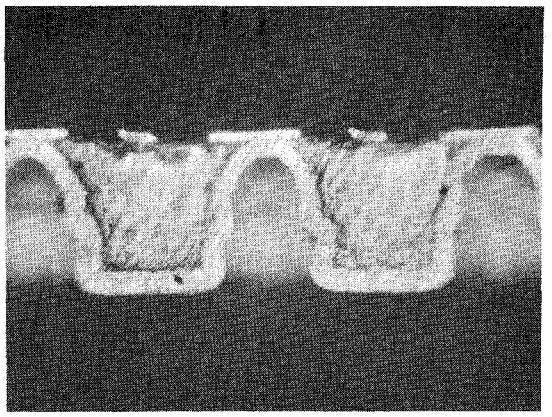

Figure 4. Via-hole Cross Section

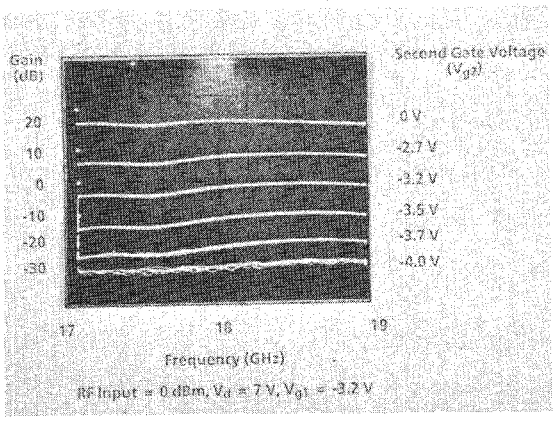

Figure 5. Measured Gain-Frequency Response